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Fabrication of Vertical Light Emitting Diode Based on Thermal Deformation of Nanoporous GaN and Removable Mechanical Supporter

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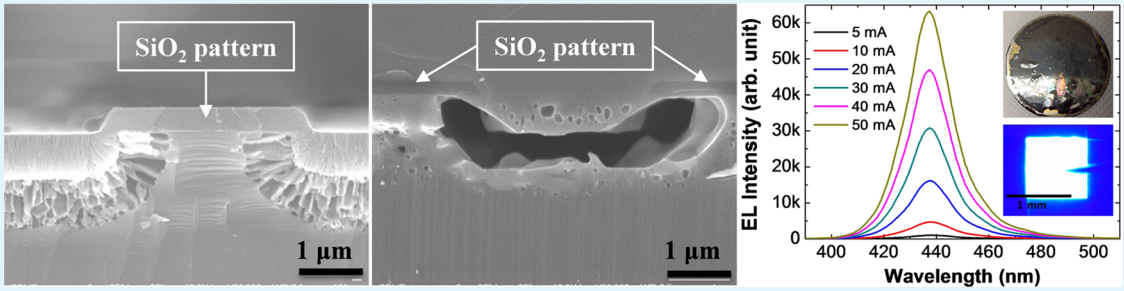

ABSTRACT: A GaN vertical light emitting diode (LED) based on the novel lift-off method was demonstrated by high temperature regrowth over nanoporous (NP) GaN template formed by electrochemical (EC) etching. A two-step EC etching process was employed on a SiO_2 patterned GaN surface to fabricate a nanoporous template with a controlled porosity profile, which enabled better structural stability than a single NP GaN. During the regrowth of LED structures, the high porosity GaN layer produced large coalesced voids due to the thermal deformation of nanopores. LED layers were then separated from the sapphire substrate and transferred to a Mo substrate by the removal of the SiO_2 mechanical supporters that held the LED structure to suppress cracks and damage during the process. The vertical LEDs fabricated using this technique showed improved optical power emission as well as low series resistance.

KEYWORDS: *vertical light emitting diode, lift-off, GaN, nanoporous, electrochemical etching, regrowth*

INTRODUCTION

GaN based III−V compound semiconductors have attracted considerable interest in optical and electrical devices such as light emitting diodes (LEDs) and high electron mobility transistors.[1−3] However, due to the lack of native substrate for GaN homoepitaxial growth, GaN and its alloys are most commonly grown heteroepitaxially on a sapphire substrate. GaN grown on a sapphire substrate was reported to contain high density threading dislocations[4,5] generated at GaN/sapphire interface because of the dissimilar lattice constants and thermal expansion coefficients between them.[6] In addition, the performance of LED was limited by poor thermal and electrical conductivities of the sapphire substrate.[7] Therefore, using conductive substrates may be beneficial for realizing an efficient current injection and thermal management properties.

The substrate separation process was previously performed by the laser lift-off (LLO) method.[8] In this method, a high power KrF excimer laser was employed to decompose the interfacial GaN into gaseous nitrogen and liquid gallium, resulting in the separation of the sapphire substrate. However, LED devices suffered from dislocations and lattice deformation in the active areas generated by high temperature and shock wave during LLO.[9] Concerning these LLO-related issues, a new technique called chemical lift-off (CLO) was developed to detach the GaN epilayer from the sapphire substrate.[10−12] For example, *n*-GaN under device layers was selectively removed laterally by electrochemical (EC) etching,[10] which led to the separation of the device structure from the substrate. Despite the several advantages of the CLO process such as low cost and no damage during the process, it is hardly commercially applicable because of the low etch rate and damage to bonding metals. Therefore, the GaN based-LED industry has demanded a new technique for obtaining free-standing GaN epilayers with simple process steps and high yield.

The shape deformation of nanopores caused by the surface migration of atoms at high temperature was studied to demonstrate the coalesced voids beneath the epitaxial structure.[13,14] Recently, based on the thermal deformation, the mechanical lift-off of GaN epitaxial layers was also developed. This lift-off process involved three main steps: (1) the formation of nanopores by EC etching, (2) the transformation of nanopores into nanovoids to reduce the structural

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stability of regrown LED epilayers by high temperature regrowth, and (3) bonding to a transfer substrate and mechanical lift-off of regrown LED layers. However, the formation of an empty space beneath the device structure significantly degraded the structural stability, which caused severe problems such as cracking and defect formation in the LED active structure.

In this work, we fabricated a vertical LED using a new lift-off method based on the shape deformation of nanopores at high temperature and selective removal of SiO_2 mechanical supporters after bonding. In this design, SiO_2 supporters hold the LED structure to suppress crack and defect formation during the process and release the LEDs after bonding by their selective removal in HF. Vertical LED chips were fabricated, and their optical and electrical properties were analyzed in detail.

EXPERIMENTAL WORK

The GaN layers used in this work were grown on a c-plane sapphire substrate by metal organic chemical vapor deposition (MOCVD). The structure consisted of a low temperature GaN buffer, a 1-μm-thick unintentionally doped GaN layer, and a 2-μm-thick n-GaN layer. A 200 nm-thick SiO_2 layer was deposited on *n*-GaN by plasma-enhanced chemical vapor deposition. SiO_2 stripe patterns of 3 μm/3 μm (mask/window) width were then fabricated by conventional photolithography and wet etching as schematically shown in Figure 1a. EC etching was carried out in 0.3 M oxalic acid at room temperature.[10] The sample was immersed in oxalic acid and biased electrically such that the sample became the anode, whereas a Pt wire immersed in the electrolyte served as a cathode. The applied voltage was varied (10 V–3 min, 16 V–4 min) to produce different porosity steps during the EC etching (Figure 1b).

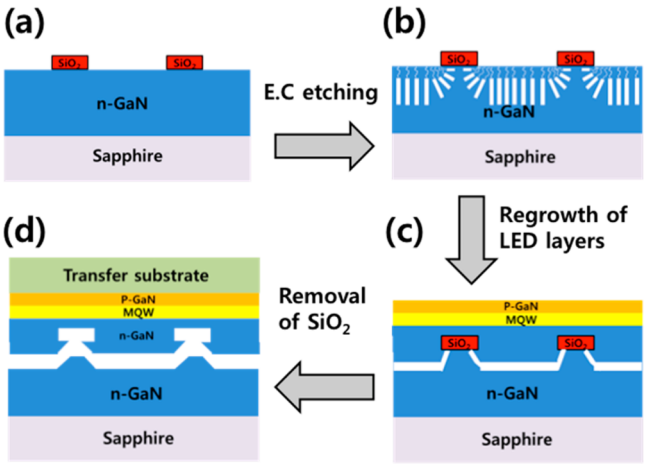

Figure 1. Conceptual process flow of epitaxial lift-off starting from (a) patterned SiO_2 on *n*-GaN, (b) EC etching, (c) the regrowth of LED layers, and (d) wafer bonding and the release of LED structures by removing SiO_2.

After careful cleaning, the NP GaN sample was reloaded into the MOCVD reactor for growth of the LED structure, consisting of *n*-GaN (3 μm), 5 pairs of InGaN/GaN multiquantum wells (MQWs), and p-type GaN (1 μm). During the high temperature regrowth of *n*-GaN, the high porosity layer was transformed into a large void and the low porosity layer was sealed through the surface diffusion of atoms. The LED structure was then bonded to a metal (Mo) transfer substrate after the deposition of metal films (Ni/Au/Sn/Au) by Au/Sn eutectic bonding. The lift-off of the LED structure from the sapphire substrate was performed by removing the SiO_2 mechanical supporter in HF at 90 °C as shown in Figure 1d. Lifted-off LEDs on the metal substrate were diced in two different sizes (250 × 250 μm^2 and 1 × 1 mm^2) using a diamond saw for preparing the LED chips. Device performance of LEDs was characterized by electroluminescence (EL), voltage–current (*V*–*I*), and optical power–current (*L*–*I*) measurements.

In order to compare the device performance of a vertical LED (V-LED) with a conventional LED, lateral LEDs (L-LEDs) were fabricated with the same growth condition of *n*-GaN, MQW, and p-GaN without the lift-off. For the L-LED process, a Ni/Au (3 nm/5 nm) current spreading layer was deposited on top,[15] which was the only difference in the layer structure from V-LED. N-type contact was made on *n*-GaN after the reactive ion etching of the *n*-metal pad. The L-LED was then diced into chips of the same sizes with V-LED.

RESULTS AND DISCUSSION

Figure 2a shows a typical SEM cross sectional image of NP GaN after EC etching. The low and high porosity layers in GaN were formed between SiO_2 patterns using two-step etching (10 V, 16 V) and the porosity of GaN was changed with the applied voltage. The procedure of forming NP GaN by EC etching has been previously reported.[10,16] The voltage applied to GaN anode produced holes at the surface by tunneling of valence electrons, resulting in oxidation etching of GaN. The etching morphology was known to depend on anodic voltage and doping concentration. Consequently, we could control the etching morphology of GaN by varying voltage for the grown sample. The deposited SiO_2 patterns at the surface of GaN deformed the propagation behavior of the nanoporous etching around the SiO_2 from a vertical to a horizontal direction. Figure 2b shows a schematic view of the effect of the patterned SiO_2 mask on the carrier depletion under reverse bias, where it modified the electric field near its edge. After the EC etching process, the high porosity layer became mechanically weak, which could cause spontaneous lift-off of the top layer, but areas below the SiO_2 mechanical supporters were protected as shown in Figure 2a. The low porosity layer was connected to the substrate through the SiO_2 pattern, which offered high structural stability after EC etching as well as after regrowth.

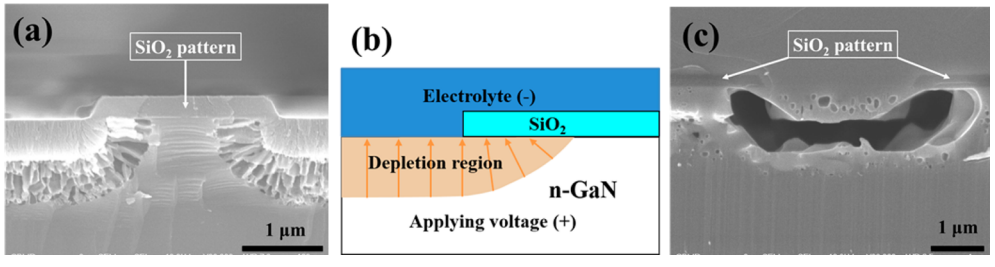

Figure 2. Cross-sectional SEM images of (a) nanopores after EC etching and (c) coalesced voids after regrowth. (b) Schematic drawing of the depletion region and electric field at the interface between the electrolyte and *n*-GaN.

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The structural stability could be controlled by increasing the thickness of the SiO_2 supporter and contact area between the low porosity layer and SiO_2.

Shape deformation of nanopores was induced by surface atomic diffusion driven by the minimization of the surface energy at elevated temperature. As discussed in the theory of Rayleigh instabilities,[17] atoms diffuse down a gradient in the surface chemical potential from the larger curvature region toward the lower curvature region of the cylindrical surface. In this study, the shape deformation of nanopores was accomplished through the high temperature GaN regrowth on the NP GaN template. N-GaN was regrown on NP GaN at 1090 °C for 105 min (3 μm GaN growth) and layers for the LED structure were then sequentially grown. During the regrowth, cylindrical pores were transformed into spherical voids, keeping the volume of the cavity unchanged.[16,18−20] Therefore, after the shape deformation, the spherical void was connected to the neighboring voids, and it eventually formed an empty space in GaN as shown in Figure 2c. The high porosity layer was transformed into a large void between the SiO_2 patterns, while low porosity GaN was nearly sealed through surface diffusion.

The high porosity layer formed by two-step EC etching led to the formation of an empty space without the appearance of pillars, which were difficult in the conventional single step EC etching process. In some papers, a certain number of nanopillars were necessary for preventing spontaneous lift-off of the regrown layer, but too many pillars were disadvantageous for clear lift-off after wafer bonding.[16,21] However, in this study, the regrown LED structure was supported by patterned SiO_2 stripes that could eliminate the need for the nano pillars. This allowed more flexibility over the regrowth condition and a higher yield of the LED process. In addition, SiO_2 patterns may possess two additional benefits: (1) enhanced crystal quality of regrown LED layers due to threading dislocation bent around the SiO_2 pattern[22,23] and (2) reduced strain of the regrown GaN layer with air voids.[16]

In order to demonstrate the wafer scale lift-off of the LED structures from the sapphire substrate, the LED wafer was bonded to a foreign metal substrate by Au/Sn eutetic bonding and was then immersed in HF at 90 °C for 3 h. During HF treatment, the LED structure formed on the 2-in. wafer was spontaneously lifted off from the sapphire by the removal of SiO_2 mechanical supporters. It is worth mentioning that after the lift-off of the LED layers, there was a remaining GaN layer on the sapphire substrate with the thickness of ∼1.5 μm, hereafter called the base GaN substrate.

Figure 3 shows SEM images displaying the microscopic surface roughness for the bottom face of lifted-off GaN and the top surface of base GaN substrate. The insets show the wafer scale lift-off of the LED layers and the remaining base GaN substrate. Both the lifted-off GaN and base GaN displayed a nanoscale roughened surface between the SiO_2 stripes, which was formed by the thermal deformation of nanopores during the regrowth. The rough surface of the lifted-off GaN combined with the trace of SiO_2 patterns will be advantageous to increase light extraction efficiency by hybrid micro/nano patterns.[24] In addition, the base GaN substrates can be recycled for repetitive growth and subsequent lift-off of LED layers by this route, offering the great reduction of substrate cost even for expensive and high quality GaN substrates.

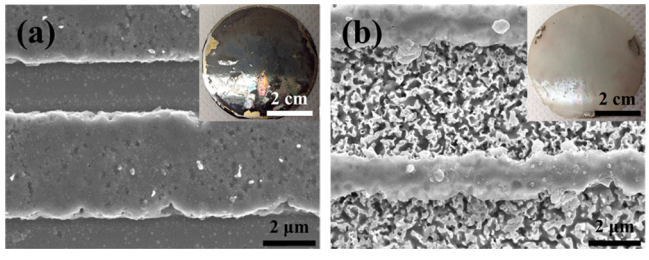

Figure 3. Plane-view SEM images of (a) the bottom face of lifted-off GaN and (b) the top surface of base GaN substrate. The insets show corresponding optical images of the 2-in. wafer.

The strain states of both the lifted-off GaN layer and the base GaN substrate were investigated by Raman spectroscopy. Figure 4 shows that the Raman peak shifts of the E_2 phonon mode for the lifted-off GaN layer and the base GaN substrate were 569.0 and 567.4 cm^{-1}, respectively. The Raman peak shift of the lifted-off GaN was similar to that of a fully strain relaxed GaN layer, which was attributed to the regrowth on the coalesced voids and the release from the substrate. On the other hand, the base GaN substrate exhibited smaller amounts of stress (0.36 GPa) than that of the as-grown GaN (0.83 GPa)[16] on the sapphire substrate. This reduced strain would have originated from the nanoscale roughened surfaces formed by the thermal deformation of the nanopores and the coalescence of the voids, as depicted in Figure 3b. Furthermore, the low strain and rough surface of the base GaN may enable the growth of high quality GaN,[25] which will allow better performance LEDs by base GaN recycling.

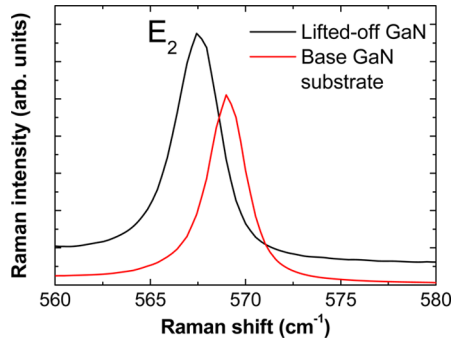

Figure 4. Raman spectra of E_2 mode of lifted-off GaN and base GaN substrate.

Figure 5a shows the measured V−I characteristics of large chip (1 × 1 mm^2 area) V-LED and L-LED. V-LED had ∼5 times lower series resistance than the L-LED due to its vertical current flow geometry and improved p-Ohmic contact resistance. The low series resistance helped to suppress the current crowding effect and to reduce heat generation in the LED chip. Figure 5b shows the room temperature EL spectra and optical image of large chip V-LED. The peak emission wavelength of V-LED was around 438 nm and slightly blue-shifted with the injection current that was caused by the band filling effect in the InGaN MQW.[26] The emission pattern represented a uniform light intensity distribution over the entire chip area. This implied that negligible current crowding occurred in V-LED, which was consistent with the *V*−*I* results.

Figure 5c compares the optical power of V-LED and L-LED with different chip sizes. First, the output power was much higher for V-LED than L-LED when the chip size was fixed. For example, the large chip V-LED showed ∼16 times higher

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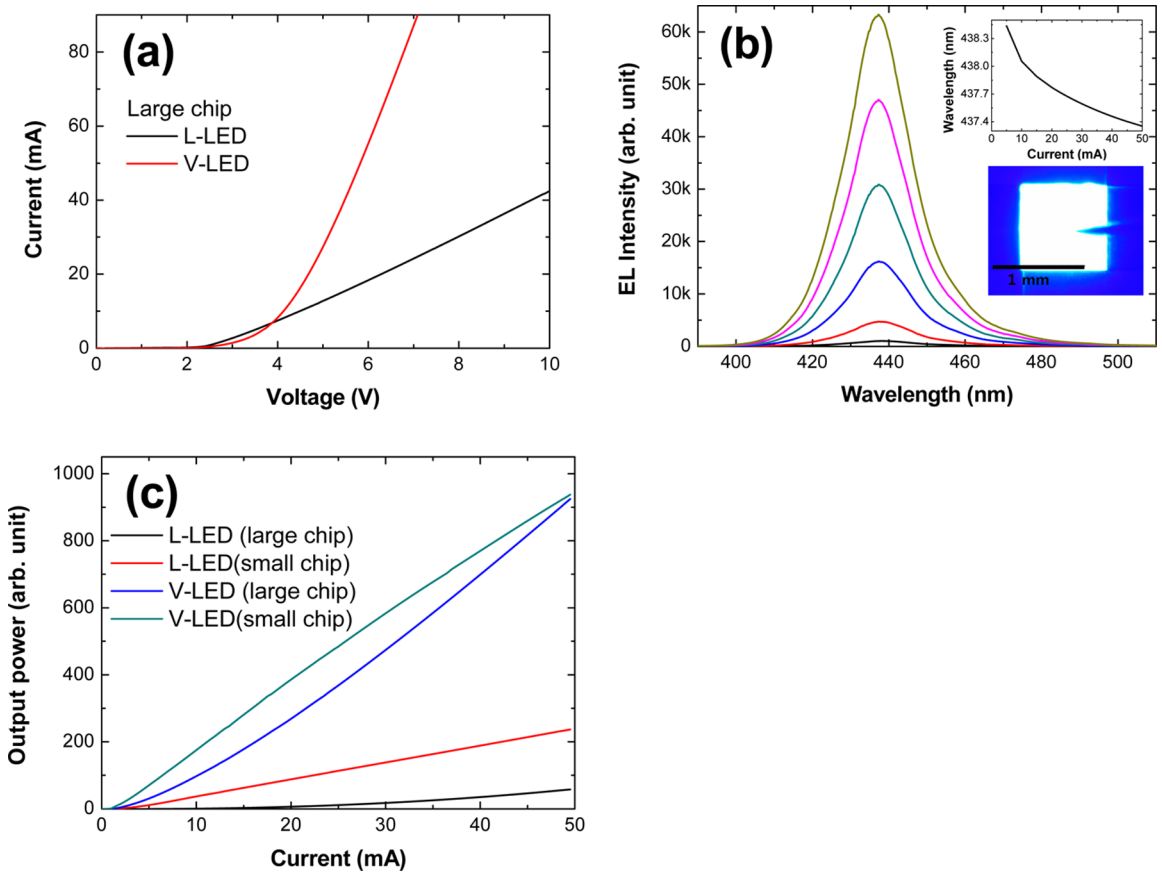

Figure 5. (a) $I-V$ characteristics of large chip L-LED and V-LED and (b) room temperature electroluminescence spectra of large chip V-LED at 5, 10, 20, 30, 40, and 50 mA. The insets are (top) the plot of emission peak wavelength vs injection current and (bottom) optical image of light emission pattern of V-LED. (c) $L-I$ characteristics of V-LED and L-LED for large and small chips.

optical emission power than L-LED at 50 mA. This indicated that V-LED had high external quantum efficiency originating from the high light extraction efficiency, fast heat dissipation, suppressed current crowding, and better epitaxial growth quality, etc.

It is interesting to monitor the chip-size dependent device efficiency for different LED structures. For V-LED, the chip area did not make a considerable difference in $L-I$ performance; however, for L-LED, the large chip showed severe optical power degradation compared to the small chip (250×250 μm^2). This behavior could be explained by the limiting factor of the device performance for each structure. Because of the flat surfaces, L-LED had narrow escape cones for top and sidewall light extractions. With larger chip dimension, the performance of L-LED was limited by light extraction from chip sidewalls and poor light extraction was obtained. The contribution of sidewall light extraction diminished with the chip size because the light power contained in sidewall escape cone decrease.[27] However, V-LED showed excellent light extraction from top surface due to the roughened chip surface and the contribution of chip sidewalls might not be significant. The light extraction efficiency of V-LED did not degrade with the chip size.

In addition, the optical power reduction of the large chip was decreasing with the operation current for V-LED. This was observed in V-LED because it has high light extraction efficiency, even for the large chip. Therefore, the suppression of efficiency droop by the low carrier density was more dominant with the increase of the operation current. This behavior demonstrated that V-LED fabricated using this technique is promising for high efficiency and high power LED production for solid state lightings or other advanced applications.

CONCLUSION

In conclusion, we fabricated GaN-based V-LED chips on a metal substrate using the lift-off method based on thermal deformation of nanopores during the regrowth of LED structures with the aid of SiO_2 mechanical supporters. SiO_2 patterns protected the low porosity GaN layer from lift-off during EC etching, while the high porosity GaN layer was transformed into coalesced voids at high temperature. After bonding to a metal substrate, LED full structures formed on a 2-in. sapphire wafer were separated by removing the SiO_2 supporters via etching in HF acid. Because of the high extraction efficiency of V-LEDs caused by hybrid micro/nano patterns, V-LEDs showed huge improvement of light output power over L-LEDs. We believe that this lift-off process could produce economical V-LED chips with greatly improved device performances.

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Notes

The authors declare no competing financial interest.

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